REMARKS

In response to the non-final Office Action of May 7, 2004, claims 1-35 have been cancelled and new claims 36-55 have been added.

In paragraph two on page 2 of the Office Action, claims 1, 6-8, 13-15, 20-22, 24-26, 28-30 and 33-35 were rejected under § 103(a) over Burkhardt, Jr. et al. (U.S. Patent No. 5,142,683) in view of Ogawa et al. (U.S. Patent No. 6,237,108). In paragraph three on page nine of the Office Action, claims 2-3, 5, 9-10, 12, 16-17 and 19 were rejected under § 103(a) over Burkhardt, Jr. et al. in view of Ogawa et al. and further in view of Suh et al. (U.S. Published Application No. 2002/0161536) and Peterson et al. (U.S. Patent No. 6,665,673). In paragraph four on page 13 of the Office Action, claims 4, 11 and 18 were rejected under § 103(a) over Burkhardt, Jr. et al. in view of Ogawa et al., Suh et al., and Petersen et al., and further in view of Urui et al (JP 61196613). In paragraph five on page 15 of the Office Action, claims 23 and 31-32 were rejected under § 103(a) over Burkhardt, Jr. et al. in view of Ogawa et al. and further in view of Suh et al. In paragraph six on page 16 of the Office Action, claim 27 is rejected under § 103(a) over Burkhardt, Jr. et al. in view of Ogawa et al. and further in view of Lai et al.

The Office Action stated that Burkhardt, Jr. et al. disclose memory 111, service agent 121 and service agent 121. The Office Action stated that service agent 121 acts as read controller and a write controller as recited in Applicant's claims. The Office Action admits that Burkhardt, Jr. et al. fail to disclose that the host processor is bypassed. Nevertheless, the Office Action stated that Ogawa teaches a DMA controller in a processor module to communicate with a shared memory.

Applicant respectfully traverses the rejections. However, in order to expedite prosecution, Applicant has cancelled claims 1-35 and added new claims 36-55. Applicant respectfully submits that new claims 36-55 are patentable over the cited references.

Burkhardt, Jr. et al. merely disclose another synchronous communication protocol between processors or devices/agents. In Burkhardt, Jr. et al., a main processor includes common memory that is accessible by an auxiliary processor. Synchronization logic is used for synchronizing and controlling message communication among multiple processors connected to the work station system bus 27. Access to the system bus 27 is controlled by a circuit 60, which

halts instructions or requests until the bus has been physically granted to the LAN interface module 16. To communicate, a sending processor interrupts the receiving processor which, in response to the interrupt, scans the mailboxes of common memory 111 to find the mailbox with its address therein thereby receiving the message. Thus, Burkhardt, Jr. et al. fail to suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Rather, Burkhardt, Jr. et al. teach away from asynchronous communications via direct memory accessing by using an interrupt scheme which places a burden on the processors. This burden is exactly what Applicant's invention is designed to prevent.

In addition, Burkhardt, Jr. et al. fail to suggest that service agent 121 asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access. Rather, according to Burkhardt, Jr. et al., service agent 121 also requires circuit 60 to authorize access to the system bus 27.

Ogawa fails to remedy the deficiencies of Burkhardt, Jr. et al. Ogawa merely teaches direct memory accessing so that a processor can communicate with a shared memory. However, Ogawa fails to disclose, teach or suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Ogawa also fails to disclose, teach or suggest asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access.

Suh et al., Peterson et al., Urui et al. and Lai et al., alone or in combination, fail to remedy the deficiencies of Burkhardt, Jr. et al. and Ogawa. Suh et al. merely teaches a polling clock. Peterson et al. merely teaches a frame invalid molecule. Urui et al. merely teaches polling memory at a required time. Lai et al. merely teaches using interrupt signals to signal a processor. However, Burkhardt, Jr. et al., Ogawa, Suh et al., Peterson et al., Urui et al. and Lai et al., alone or in combination, fail to disclose, teach or suggest a read controller that determines when a host command has been provided to a host memory and asynchronously retrieves the host command directly from a host memory via direct memory access. Burkhardt, Jr. et al., Ogawa, Suh et al., Peterson et al., Urui et al. and Lai et al., alone or in combination, also fail to disclose, teach or

suggest asynchronously signaling a successful command transfer from the host memory to the host messaging unit via direct memory access.

Therefore, Applicant respectfully submits that new claims 36-55 are patentable over the cited references.

On the basis of the above amendments and remarks, it is respectfully submitted that the claims are in immediate condition for allowance. Accordingly, reconsideration of this application and its allowance are requested.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Attorney for Applicant, David W. Lynch, at 651-686-6633 Ext. 116.

Respectfully submitted,

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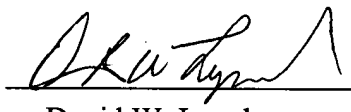
By: 

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